From December 2008 *High Frequency Electronics*

Simulating and Designing a PLL Frequency Synthesizer for GSM Communications

By Samir Kameche, Mohammed Feham, University of Tlemcen,
and Mohamed Kameche, Center of Space Techniques, Algeria

Here is a case history describing the design process, including selection of components based on their effects on the PLL's noise characteristics

Phase locked loops (PLL) are used in almost every communication system. Some of the uses include recovering clock from digital data signals, performing frequency, phase modulation and demodulation, recovering the carrier from satellite transmission signals and as a frequency synthesizer. It is very well known that there are many designs in communication that require frequency synthesizers to generate a range of frequencies; such as cordless telephones, mobile radios and other wireless products. The accuracy of the required frequencies is very important in these designs as the performance is based on this parameter. Using crystal oscillators to generate frequency is not only impractical, but it is impossible to use many crystal oscillators for multiple frequencies. In the last decade, most frequency synthesizers are based on the PLLs, regarding their advantages as minimum complex architecture, low power consumption and integration technology possibilities. In practice, there are three basic types of frequency synthesizer: direct frequency synthesizer, direct digital frequency synthesizer and indirect frequency synthesizer. The indirect frequency synthesizer has advantages over the other two types, including low power consumption, low phase noise, and high stability [1]. Considering the scope of this single circuit, this work is devoted to the design of an indirect frequency synthesizer that can be applied to GSM communications. In the simulation, we include the phase noise in each component in the circuit, and we discuss the reference spurs and their effect on the noise performance of the PLL frequency synthesizer. The success of this design depends crucially on the accuracy of the values calculated for the loop filter. In our case, the loop filter is accurately evaluated by using an efficient estimation technique.

Design and Theory

The basic phase-lock-loop configuration considered in the design is shown in Figure 1. The PLL consists of a high stability crystal reference oscillator, a frequency synthesizer, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, and programmable frequency dividers. A passive filter is desirable for its simplicity, low cost, and low phase noise.

In the loop, a low pass filter is incorporated in order to suppress spurs produced in the phase detector and to avoid unacceptable frequency modulation in the VCO [2].

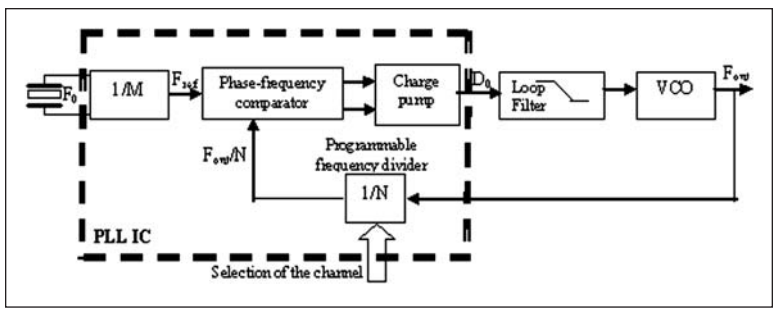

Figure 1 · Block diagram of the designed frequency synthesizer.

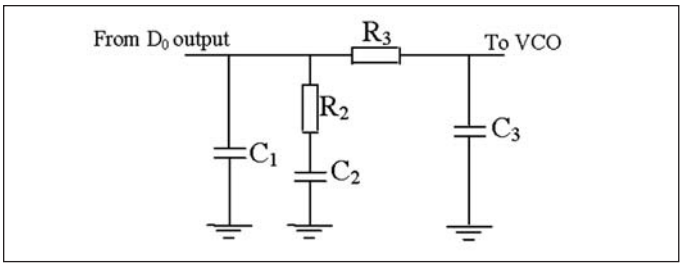

Figure 2 · Loop filter circuit.

Figure 2 shows the standard third order loop filter used in such circuits. This comprises a second order filter section and a *R3–C3* section providing an extra pole to assist the attenuation of the sidebands that appear at multiples of the comparison frequency.

The transfer function of the loop filter in Figure 2 is given by

$$Z_{fil3} = \frac{Z(s).\left(\frac{1}{C_3.s}\right)}{Z(s). + R_3 + \left(\frac{1}{C_3.s}\right)} \tag{1}$$

where *Z(s)* describes the transfer function of the second order loop filter, as given by

$$Z(s) = \frac{s.C_2.R_2 + 1}{s^2 C_1.C_2.R_2 + s.C_1 + s.C_2} \tag{2}$$

The open loop transfer function is defined as the transfer function from the phase detector input to the output of the PLL. Note that the VCO gain is divided by a factor of *s*. This is to convert output frequency of the VCO into a phase. The open loop transfer function is shown below

$$G(s) = \frac{K\phi Kvco.Z(s)}{s.N} \tag{3}$$

The closed loop transfer function takes into account the whole system and does not assume that the phase of one of the phase detector inputs is fixed at a constant zero phase.

$$K(s) = \frac{G(s)}{1 + G(s).N} \tag{4}$$

The transfer function in (4) involves an output phase divided by an input phase. By considering the change in output frequency produced by introducing a test frequency at various points in the PLL loops, all of the transfer functions can be derived.

As mentioned in the introduction, in order to guarantee accurate results for the design, the effect of the noise in each component in the circuit is introduced in the simulation. First, the noise in the reference oscillator is amplified by the gain of the closed loop transfer function. A simple approximation for this source of noise due to the reference crystal itself, as with any oscillator, is inversely proportional to the offset frequency. Higher order approximations can be used but the experience has demonstrated that the 1/*f* approximation is a good starting point for this study.

If a temperature compensated crystal oscillator (TCXO) is employed, phase noise data should be obtained from the manufacturer so that reference values can be used with the models.

The noise in the reference oscillator, $N_{tcxo(f)}$, is expressed by [3]

$$N_{tcxo}(f) = \frac{10\left(\frac{N_{tcxo\_ref}}{20}\right)}{\frac{f}{f_{tcxo\_ref}}}.\left(K(f).\frac{1}{R}\right) \tag{5}$$

The reference spurs are also introduced in the simulation. The powers of these spurs are calculated by the closed loop transfer function evaluated at the spur offset frequencies, F_{spur}. In several studies, F_{spur} is assumed to be a multiple of the comparison frequency, F_{comp}.

The power of the reference spur is expressed by [4]

$$Spur_{Gain}\left(F_{Spur}\right) = 20\log\left[\frac{K_{VCO}Z(s)K\phi}{s}\right] \tag{6}$$

The VCO noise can be modeled as a simple approximation inversely proportional to offset frequency from the carrier. The noise of the VCO is effectively high-pass filtered by the PLL providing rejection of phase noise or phase error within the bandwidth, but leaving VCO noise well outside of the loop bandwidth unaffected. The VCO noise is given by [5]

$$Nvco = Kvco + \frac{Kvco_2}{f^2} + \frac{Kvco_3}{f^3} \tag{7}$$

Results and Discussion

The phase-locked loop allows stable high frequencies to be generated from a low-frequency reference. Any system that requires stable high frequency tuning can benefit from the PLL technique. A good example of a PLL

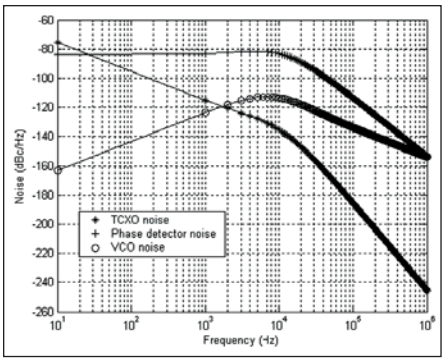

Figure 3 · TCXO, phase detector and VCO noise.

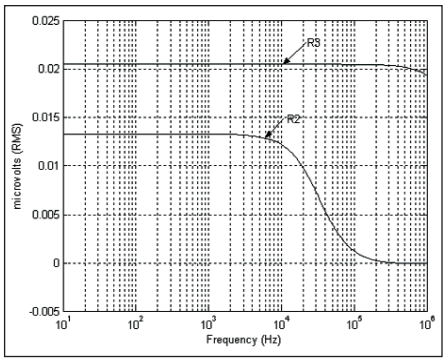

Figure 4 · Noise in resistors versus frequency.

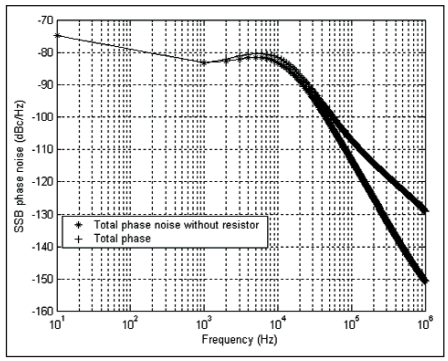

Figure 5 · SSB phase noise with and without resistor noise

application is a GSM handset or base station. Moreover, an extended GSM (EGSM) system with only 10 MHz between the transmission band and reception band can be supported simply by extending the frequency band.

The handset has a transmit (Tx) range of 880 MHz to 915 MHz and a receive (Rx) range of 925 MHz to 960 MHz. Conversely, the base station has a Tx range of 925 MHz to 960 MHz and an Rx range of 880 MHz to 915 MHz. For this example, we will consider just the base station transmit and receive sections.

The essential component used to realize the PLL is a frequency synthesizer capable to generate and to control a very stable signal with a low noise in the frequency range of 500 MHz to 1.2 GHz. The voltage controlled oscillator used in this application is capable to generate a power of +8.6 dBm into a load of 50 ohms. Its tuning linearity is relatively good (21-36) MHz/V. We note that the linearity is very important to determine the loop filter parameters. Also, this VCO presents a pulling of 5 MHz, a pushing of 0.6 MHz/V and a phase noise of –70, –94, –114 and –134 dBc/Hz at the offset frequencies of 1 kHz, 10 kHz, 100 kHz and 1 MHz, respectively. The crystal reference oscillator is a TCXO capable of generating a very stable frequency of 10 MHz with a phase noise of –110 dBc at an offset frequency of 10 kHz. The PLL can be programmed via a laptop computer and parallel port cable.

Figures 3, 4 and 5 illustrate, respectively, the phase noise in each component (TCXO, phase detector and VCO), noises generated by resistances and the total noise without and with the noise generated by resistances. We note that the references spurs are not included in the total noise shown in Figure 5. The results show that inside the loop bandwidth (10 Hz to 10 kHz), the noise level of the reference oscillator is more significant owing to the fact that the gain of the closed loop transfer function is high in this band and falls off quickly outside.

The results also show that the resistor noise contribution is very small at the synthesizer output.

In order to demonstrate that the noise of the VCO is highly filtered by the PLL, by rejecting the phase noise or error of phase in the bandwidth, Figure 6 exposes the loop error response. This function is obtained by association between the open and closed loop responses.

In this work, the choice of the loop filter is a very critical part of the synthesizer circuit. In general, a low loop filter cut-off frequency does not attenuate the phase noise much, but it makes the PLL's response slower, increasing the time to change frequency (PLL lockup time), but it suppresses the references spurs. Conversely, a high cut-off frequency provides faster PLL response, shorter PLL lockup time, while the output signal contains higher level reference spurs. Consequently we note that at the time

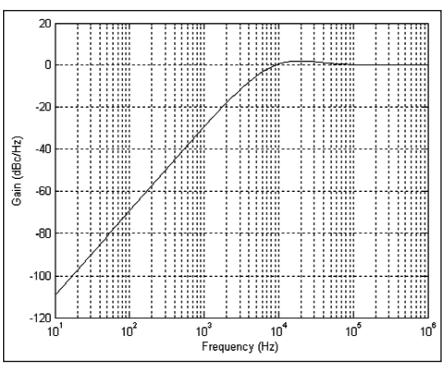

Figure 6 · Loop error response.

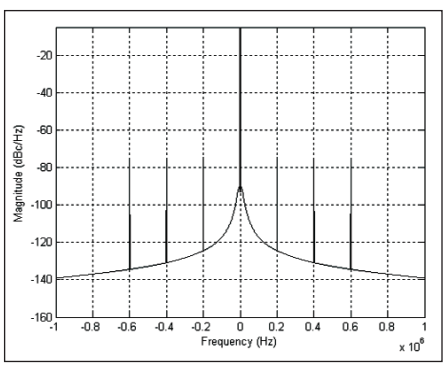

Figure 7 · PLL output spectrum.

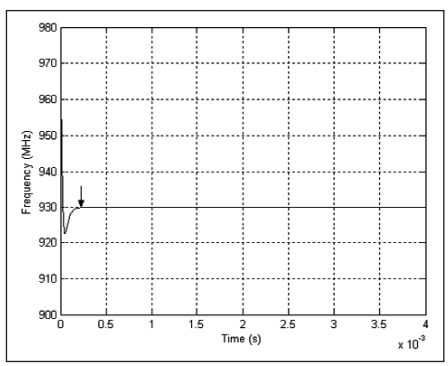

Figure 8 · PLL transient response.

when a problem is solved, another is created. This is why determining the best choice of the loop filter remains a great interest to microwave circuit designers.

An accurate estimation of the loop filter is used, which guarantees the precision of the design. The output spectrum and the transient response of a chosen loop filter design are illustrated in Figures 7 and 8. The spurious levels, the phase noise and the frequency transition are evaluated under several conditions.

The results obtained indicate a noise density of –75.4 dBc/Hz at multiples of the comparison frequency, a settling time of frequency switching (frequency change of 35 MHz) of about 250 µs, an RMS phase noise of 0.01633 rad and a signal to noise ratio (S/N) of about 35.74 dB.

Conclusion

The simulation and the design of a frequency synthesizer operating in EGSM band are presented in this paper. The present design takes into account the noise in each component and its effect on the performance system. The obtained output spectrum presents a noise density of –75.4 dBc/Hz at multiples of comparison frequency, a lockup time of 250µs, an rms phase error of 0.01633 rad and a signal on noise ratio (S/N) of 35.74 dB. These performances confirm and justify the use of such circuits in modern communication systems.

References

1. Jwo-Shiun Sun, "Design A Frequency Synthesizer for Mobile Communication Systems," *Microwave & RF,* Vol. 39, No. 11, November 2000, pp. 63-72.

2. Akihiro Kajiwara and Masao Nakagawa, "A New PLL Frequency Synthesizer with High Switching Speed," *IEEE Transactions on Vehicular Technology,* Vol. 41, No. 4, November 1992, pp. 407-413.

3. L. Lascari, "Accurate Phase Noise Prediction in PLL Synthesizers," *Applied Microwave and Wireless,* Vol. 12, No. 2, pp. 30-38, February 2000.

4. D. Banarjee, *PLL Performance, Simulation, and Design*, 2nd Edition, 2001, pp. 13-67.

5. E. Drucker, "Model PLL Dynamics and Phase-noise Performance," *Microwave & RF,* Vol. 39, No. 2, February 2000, pp. 73-82.

Author Information

Samir Kameche was born in Ghazaouet, Algeria, in 1981. He received his electrical engineering degree in electronics in 2004 and the Master degree in 2007 from the University of Tlemcen, Algeria. Since 2004, he has been with the Department of Electronics at the University of Tlemcen. His research interests include digital frequency synthesizers for microwave circuit applications. He can be reached at: kamsamir@yahoo.fr

Mohammed Feham received the Doctor-Engineer degree in optical and microwave communications from the University of Limoges (France) in 1987 and the Doctor Es-Science degree from the University of Tlemcen (Algeria) in 1996. Since 1987, he has been assistant professor and professor of microwave and communication engineering. His research interest is in computational electromagnetics, especially in the computer modeling of reciprocal and nonreciprocal microwave components (couplers, filters, novel dielectric materials, etc.). Dr. Feham has served on the scientific council and other committees of the electronic Department of the University of Tlemcen.

Mohamed Kameche graduated in Electronics from the University of Tlemcen in 1998, where he also received the Master and Ph.D degrees in Electronics (Signals and Systems) in 2001 and 2005, respectively. From 2000 to 2001, he worked in the Department of Electronics at the University of Tlemcen as an associate researcher. Since February 2002, he has been working with Instrumentation Division in the Centre of Space Techniques (CTS) at Arzew, Oran, Algeria. His research interests are temperature effects on RF and microwave devices and package modeling for space microwave circuit applications.